IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. MA-002-3

In re patent application of

Andrew J. WALKER et al.

Serial No. 09/927,642 Group Art Unit: 2829

Filed: August 13, 2001 Examiner: Evan T. Pert

For: NONVOLATILE MEMORY ON SOI AND COMPOUND SEMICONDUCTOR SUBSTRATES AND METHOD OF FABRICATION

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

To the Commissioner:

This Appeal Brief is being filed in triplicate together with authorization to charge deposit account 502302 for the appeal fee and a one-month extension of time. Appellants hereby appeal the final rejection of claims 1-12, 19, 20 and 69 in the Office Action of August 21, 2003 ("Office Action") in the above-identified application to the Board of Patent Appeals and Interferences.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria VA 22313-1450 on the date below.

Pamela J. Squyres, reg. no. 52,246
Printed Name

Signature

2/20/04
Date of Deposit

REAL PARTY IN INTEREST

The real party in interest is Matrix Semiconductor, Inc., a Delaware corporation.

RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals and interferences.

STATUS OF CLAIMS

Claims 1-70 are pending. Non-elected claims 13-18, 21-24, and 27-68 have been withdrawn from consideration. Claims 25-26 are allowed. Claim 70 was withdrawn by the Examiner. Claims 1-12, 19, 20 and 69 have been finally rejected under 35 USC § 103.

A listing of the pending claims is presented in the APPENDIX.

STATUS OF AMENDMENTS

No amendments after final rejection were filed.

SUMMARY OF INVENTION

Digital memory is either volatile or nonvolatile. Volatile memory retains stored data as long as power is supplied to the memory, and loses data when power to the device is turned off. Nonvolatile memory retains information even when power is removed. Volatile memory in general allows faster access times, while nonvolatile memory is slower.

The present invention is a nonvolatile memory array. In preferred embodiments, the nonvolatile memory array is a monolithic three dimensional memory array of stacked memory levels formed above a substrate. The first memory level is formed using standard semiconductor fabrication technology, including deposition, photolithography, and etch. Using planarization techniques, for example chemical mechanical planarization (CMP), a relatively planar surface is formed on the first memory level, upon which a second memory level is formed, stacked above the first, again using standard technology. Multiple memory levels can be stacked in this way.

Various embodiments of such a memory array are described in the present application, having memory cells which are PROMs, EPROMs, or EEPROMs.

Semiconductor devices, including memory arrays, are typically formed on a semiconductor substrate, which is most typically a bulk monocrystalline silicon wafer.

Conventional memory devices are formed in such a monocrystalline silicon substrate, in which the monocrystalline silicon of the substrate forms a portion of the device, such as the channel of a transistor. In contrast, the memory cells of the present invention comprise polysilicon and are vertically stacked above the substrate. Devices formed in polysilicon in general are cheaper and slower than devices formed in monocrystalline silicon. Vertically stacking the memory levels greatly increases the amount of memory that can be formed over a given substrate area, also tending to decrease cost. The nonvolatile memory array of the present invention is a relatively slow, relatively low-cost device.

Memory cells must be written and read (and erased, if the cells are rewriteable.) Driver circuitry is typically associated with a memory to do this. In embodiments of the present invention, the driver circuitry is formed in the substrate (unlike the memory cells, which, as noted, are stacked above the substrate, above the driver circuitry.)

The present invention describes forming a nonvolatile memory array using a silicon-on-insulator (SOI) substrate rather than a conventional monocrystalline silicon substrate, and, in preferred embodiments, forming the driver circuitry in the SOI substrate.

An SOI substrate is either a three-layer or a two-layer structure. The SOI substrate includes a silicon layer formed on an insulator. In the three-layer versions, the insulator is a thin insulating layer, itself formed on a substrate such as monocrystalline silicon. In the two-layer versions, the silicon layer is formed on an insulating substrate. In the present invention the driver circuit is located in the silicon layer at the top of this two- or three-layer structure.

Various techniques are known for forming an SOI substrate. All result in a silicon layer on an insulator. Depending on the method of formation, the silicon layer can be single-crystal, polycrystalline, or amorphous. The substrate can be monocrystalline silicon (with an intervening insulator) or some insulating material, such as glass, plastic, or ceramic.

Perhaps the best known method to form an SOI substrate is the SIMOX (separation by implantation of oxygen) method, which includes providing a monocrystalline silicon substrate, implanting oxygen below the surface of the substrate, then annealing. After anneal, a thin single crystal silicon layer remains above the silicon oxide layer.

Alternatively, an SOI substrate may be formed by a seeded lateral epitaxy method. In this method, an insulating layer is formed over a monocrystalline silicon substrate. One or more windows to the substrate are formed in the insulating layer. A silicon layer is deposited over the insulating layer, such that it contacts the substrate through the windows in the

insulating layer. The silicon layer may be deposited as a single crystal silicon layer over the silicon oxide layer using the substrate as a seed. Alternatively, the silicon layer may be deposited as an amorphous or polycrystalline silicon layer, and then recrystallized by laser or thermal annealing into a single crystal layer using the substrate as a seed. Both this method and the SIMOX method yield a single-crystal silicon layer over an insulating layer, the insulating layer over a monocrystalline substrate.

Alternatively, the silicon layer formed on the insulating substrate may be a single crystal silicon layer formed by the wafer bonding method. This method begins by forming driver circuitry in a temporary bulk monocrystalline silicon substrate. The temporary substrate is then selectively removed from below the driver circuitry, such that only the single crystal silicon layer in which the driver circuit is located remains. The temporary substrate is then removed, leaving the driver circuit in its thin layer of single crystal silicon. A permanent insulating substrate (such as a glass, plastic, or ceramic) is attached to the thin single crystal silicon layer containing the driver circuitry. This method forms a single crystal layer containing driver circuitry on an insulating substrate of glass, plastic, or ceramic.

Another method to form an SOI substrate is to deposit a polycrystalline silicon or an amorphous silicon layer formed on an insulating layer or on an insulating substrate. The crystallinity of the deposited silicon layer may be improved by laser and/or thermal annealing, or a crystallization catalyst material, such as Ge, or a transition metal, such as Ni, Pt, Pd, etc., or their silicides, may be used as a seed for the crystallization of an amorphous silicon layer. This method of producing an SOI substrate is distinct from the others in that the silicon layer is polycrystalline or amorphous rather than single-crystal. A nonvolatile memory array having driver circuitry formed in such a polycrystalline silicon SOI substrate is recited in claim 6.

The SOI substrates formed by these various techniques have different properties, costs, and appropriate uses.

ISSUES

There are two issues presented in this appeal:

I. Whether claims 1-5, 7-12, 19, 20 and 69 are unpatentable under 35 USC §103(a) over U.S. Patent 5,835,396 ("Zhang") in view of an article entitled "Active Body-Bias SOI-CMOS Driver Circuits" ("Wada et al.").

II. Whether claim 6 is unpatentable under 35 USC §103(a) over Zhang in view of Wada et al.

GROUPING OF CLAIMS

I. Group I: claims 1-5, 8-12, 19-20 and 69 stand or fall together.

II. Group II: claim 6

Group II (claim 6) is separately patentable over Group I because claim 6 recites a polycrystalline silicon layer over an insulating layer.

SUMMARY OF THE ARGUMENT

The claims of Group I are patentable over Zhang in view of Wada et al. because neither reference teaches or suggests use of SOI in such a memory array. Use of SOI was not standard for use in nonvolatile memory arrays at the time of invention because of cost.

The claims of Group II are patentable over Zhang in view of Wada et al. because neither reference teaches or suggests use of SOI having a polycrystalline silicon layer, and the Examiner has not identified a motivation to use such an SOI substrate.

ARGUMENT

The § 103(a) Rejections Should be Reversed

A. Claim 1 is Patentable Over the Applied References

Independent claim 1 recites a nonvolatile memory array, comprising an array of nonvolatile memory devices; at least one driver circuit; and a substrate; wherein the at least one driver circuit is not located in a bulk monocrystalline silicon substrate.

The Examiner has rejected claim 1 over Zhang in view of Wada et al. Zhang teaches a nonvolatile memory array formed over a "semiconductor substrate" (col. 3, line 40). Zhang does not specifically name the semiconductor substrate as bulk monocrystalline silicon, though such a choice would have been standard at the time of invention, and remains so today. Wada et al. begin with this sentence: "SOI devices operate faster and consume less power than bulk ones due to their small junction capacitance." In section 2, page 3 of the Office Action, the Examiner points out that SOI was well known at the time of invention, and

maintains that it would therefore have been obvious to one skilled in the art at the time of invention to have selected SOI as the semiconductor substrate of Zhang, relying on the quoted sentence from Wada et al. as motivation.

In the summary of the invention, Appellants noted the many different varieties of SOI, which have different properties, costs, and uses. Appellants believe that Wada et al. speaks of SOI formed according to a method which creates a single crystal silicon layer over an insulating layer, such as the SIMOX, seeded lateral epitaxy, or wafer bonding methods. Appellants base this assumption on the improved device characteristics claimed by the reference, which simply do not apply when the silicon layer is polycrystalline, and to reference [2] of Wada et al., titled "A 0.5V SIMOX-MTCMOS Circuit with 200 ps Logic Gate," implying use of the SIMOX method.

Further, Appellants have attached as Exhibit A an article from the *EE Times*, a widely read industry journal, regarding use of SOI. The article, entitled "Better models, production methods expand SOI applications," was published in September, 2002, about one year after filing of the present application. The article states: "Today, two SOI manufacturing methods are used for producing the vast majority of wafers: separation by implantation of oxygen (SIMOX) and wafer bonding." Both methods produce a single crystal silicon SOI substrate.

Appellants do not contest that SOI was generally known at the time of invention. The mere fact that a technology is known, though, hardly makes it an obvious choice for every use in any related field. Techniques to enhance performance in race car engines, for example, may be known to those involved in automotive design, but this doesn't automatically make those techniques obviously relevant for use in a tractor engine.

As noted in Wada et al., single-crystal silicon layer SOI devices in general operate faster and consume less power than bulk ones. Single-crystal silicon SOI substrates yield better devices; therefore, absent other considerations, one would expect single-crystal SOI to simply supersede bulk monocrystalline silicon as the usual substrate for semiconductor devices. That single-crystal silicon SOI has not done so makes it clear that other considerations, and apparently compelling ones, must exist.

The most important consideration is cost. A single-crystal silicon SOI substrate wafer is more expensive than the standard bulk monocrystalline silicon wafer. The *EE Times* article, which discusses the advantages, disadvantages, and typical uses of SOI, summarizes:

> The cost issue is a sizable barrier for proliferation of SOI because many applications cannot command a sufficiently higher price for SOI's traditional advantages of higher speed or lower dynamic power. For this reason, SOI has mainly found use in high-speed applications, or in some cases RF applications, where the isolation properties enable a favorable cost/value scenario.

In short, use of SOI has been standard in high-speed, high-performance applications that justify the increased cost. A relatively slow nonvolatile memory array, such as the memory array of Zhang, is not such a device.

In the last paragraph of section 7 of the Office Action (page 6) the Examiner maintains that faster access and lower power is simply better, regardless of the circumstances: "Drivers (such as memory decoders) are clearly better if they are faster and more efficient because memory access is desirably as fast as possible (who wants to wait for memory access?) and power use is desirably as little as possible (who wants to spend more power?)"

If this were the case, every car would be a high-performance car and every watch a Rolex. As evidenced by the variety of options available in consumer goods, there is a tradeoff between price and performance, and consumers routinely make choices at every point along this wide spectrum.

In addition to the fact that the memory array of Zhang is one for which extra speed of single-crystal silicon SOI doesn't justify additional cost, the Examiner's contention that faster driver circuitry necessarily means better device performance is hardly self-evident. When the Examiner rhetorically asks who wants to wait for memory access, the Examiner assumes that the speed of the driver circuits limit access times. In fact, the nonvolatile memory is itself much slower than the driver circuitry, and in general the driver circuitry is waiting for the memory, not the reverse, particularly when used with standard parallel processing techniques. Just as putting a turbo-charger in a Volkswagen Beetle will not necessarily make the car go faster, faster driver circuitry resulting from use of a single crystal silicon SOI substrate may not in fact yield meaningful speed improvement.

As Appellants have pointed out why SOI is not an obvious choice for a nonvolatile memory array, it may raise the question why Appellants have chosen in the present application to teach and claim its use. Appellants were aware that unforeseen technological advances, such as a drastic decrease in the cost of SOI, occur with notorious regularity in semiconductor technology. Such an advance can quickly and unexpectedly reverse the outcome of cost-benefit calculations; thus Appellants have chosen to make the claims of the present application.

B. Claim 6 is Patentable Over the Applied References

As noted, the most common forms of SOI, which Wada et al. apparently refer to, include a single crystal silicon layer over an insulator. (To reiterate Appellants' reasons for concluding that Wada et al. refer to single crystal silicon SOI: a) The improved device characteristics claimed by the reference do not apply when the silicon layer is polycrystalline; b) the only explicit mention of a method of formation of SOI in Wada et al. is reference [2], titled "A 0.5V SIMOX-MTCMOS Circuit with 200 ps Logic Gate," implying use of the SIMOX method, which creates single crystal silicon SOI; and c) the attached *EE Times* article, which states: "Today, two SOI manufacturing methods are used for producing the vast majority of wafers: separation by implantation of oxygen (SIMOX) and wafer bonding," both of which produce a single crystal silicon SOI substrate.)

In section 2, page 4 of the Office Action, in rejecting claim 6, the Examiner says that "all known SOI substrates provide the advantages of 'faster' and 'less power' for devices in general, as disclosed and taught by Wada et al. in the first sentence of the introduction." Appellants respectfully disagree.

As described in the present application and in the summary of the invention, one method of forming an SOI substrate involves forming a polycrystalline silicon layer over an insulator. A nonvolatile memory array having a driver circuit located in a polycrystalline silicon layer, the polycrystalline layer located over an insulating layer, is recited in claim 6. As is well-known in the art, devices formed in polycrystalline silicon are generally slower and have higher leakage characteristics than those formed in monocrystalline silicon. The advantages claimed by Wada et al. cannot be assumed to apply to polycrystalline silicon SOI. Thus the Examiner's contention that improved speed and power characteristics of SOI would make it an obvious choice for the semiconductor substrate of Zhang cannot be supported

when the silicon layer of the SOI is polycrystalline, as in claim 6. The Examiner, therefore, has not supplied a plausible suggestion why the cited sentence of Wada et al. ("SOI devices operate faster and consume less power than bulk ones due to their small junction capacitance,") would provide motivation to use such a substrate in the nonvolatile memory array of Zhang.

CONCLUSION

For the reasons set forth above, Appellants respectfully submit that Claims 1-12, 19-20, and 69 are patentable over Zhang in view of Wada et al. Accordingly, Appellants respectfully solicit the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

2/20/04
Date

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APPENDIX

1. A nonvolatile memory array, comprising:
an array of nonvolatile memory devices;
at least one driver circuit; and
a substrate;
wherein the at least one driver circuit is not located in a bulk monocrystalline silicon substrate.

2. The array of claim 1, wherein the at least one driver circuit is located in a silicon on insulator substrate.

3. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over a silicon oxide layer formed by a SIMOX method.

4. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over an insulating layer formed by a seeded lateral epitaxy method.

5. The array of claim 2, wherein the at least one driver circuit is located in a single crystal silicon layer over an insulating substrate formed by a wafer bonding method.

6. The array of claim 2, wherein:
the at least one driver circuit is located in a polycrystalline silicon layer;
the polycrystalline silicon layer is located over an insulating layer; and
the insulating layer is located over a bulk monocrystalline silicon substrate.

7. The array of claim 2, wherein the at least one driver circuit is located above a monocrystalline silicon substrate.

8. The array of claim 7, wherein the at least one driver circuit is separated from the monocrystalline silicon substrate by an insulating layer.

9. The array of claim 2, wherein the at least one driver circuit is formed above a glass substrate.

10. The array of claim 2, wherein the at least one driver circuit is formed above a plastic substrate.

11. The array of claim 2, wherein the at least one driver circuit is formed above a ceramic substrate.

12. The array of claim 11, wherein the at least one driver circuit is formed in a single crystal silicon layer formed on a sapphire substrate.

19. The array of claim 1, wherein the array of nonvolatile memory devices comprises an array of PROMs, EPROMs or EEPROMs.

20. The array of claim 19, wherein the array of nonvolatile memory devices comprises a monolithic three dimensional array of memory devices.

69. A nonvolatile memory array, comprising:
an array of nonvolatile memory devices;
a silicon on insulator substrate; and
at least one memory driver circuit located in the silicon on insulator substrate.

Exhibit A

Better models, production methods expand SOI applications

By Michael A. Mendicino, Craig S. Lage, DigitalDNA Laboratories, CMOS Platform Technology Development, Motorola Corp., Austin, Texas, EE Times
September 23, 2002 (4:20 p.m. EST)
URL: http://www.eetimes.com/story/OEG20020923S0063

Silicon-on-insulator (SOI) will continue to find its place in high-performance applications and branch out into some of the networking and communications space. Scaling presents challenges for all technologies, but for SOI there is an additional burden of preserving a performance advantage relative to bulk silicon. This will necessitate thinner film SOI substrates (T, Si<50nm) for reduced capacitance, favorable coupling, and well-balanced floating-body effects.

In addition, more widespread use may occur if SOI can break the cost barrier either by substantial wafer cost reduction or by enabling a much smaller die size than could be realized in bulk silicon technologies. The latter could result from a novel system-on-chip or memory module such as the capacitorless 1T DRAM recently announced by the Swiss Federal Institute of Technology.

Thin-film silicon-on-insulator (TFSOI) is a semiconductor wafer technology that provides improved circuit speed and power relative to its bulk silicon counterpart and can possibly enable novel devices or integration.

Today, two SOI manufacturing methods are used for producing the vast majority of wafers: separation by implantation of oxygen (SIMOX) and wafer bonding. Both methods have been modified for improved quality and cost, with wafer suppliers inventing, acquiring, or adopting the full range of options. SOI material cost is high relative to bulk silicon or epitaxial wafers and can increase the fully processed wafer cost in the range of 10-20 percent. In addition, for leading-edge CMOS, there is very little die shrink due to the SOI isolation because most design rules have become lithography-limited.

The cost issue is a sizable barrier for proliferation of SOI because many applications cannot command a sufficiently higher price for SOI's traditional advantages of higher speed or lower dynamic power. For this reason, SOI has mainly found use in high-speed applications, or in some cases RF applications, where the isolation properties enable a favorable cost/value scenario. SOI transistor performance is improved over an equivalent bulk device because of the buried insulating layer in the wafer. This layer reduces the amount of electrical charge that the transistor has to move during a switching operation, making it faster and allowing it to switch using less energy (lower power).

These properties can be exploited further in circuit design through the use of higher stacked gates that would be prohibitive in bulk designs. Unfortunately, the same insulating layer that improves speed and power also bounds the body region of the SOI transistor such that its potential depends on such factors as the capacitive coupling to the gate, source/drain, substrate, and any other sources of charge generation or recombination. The body voltage directly affects the threshold voltage of the transistor and its switching characteristics, which means circuit design needs to account for these floating-body effects.

Some companies such as Motorola use internally developed compact models to accurately predict

the floating-body behavior and enable LSI circuit design, while other companies find public-domain models offer reasonable SOI predictive capability.

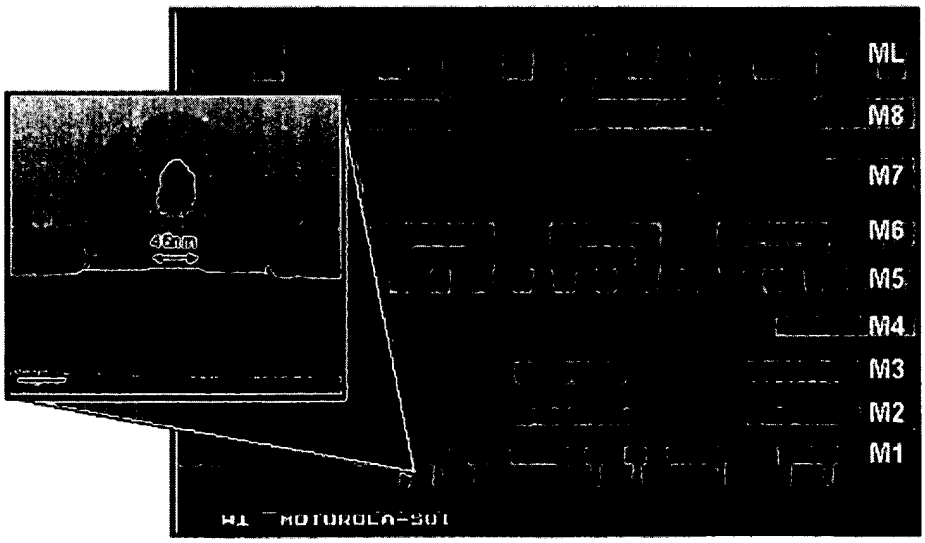
An SOI CMOS process is similar in many ways to the bulk process. Key differences are in the isolation module and transistor integration for high performance while managing floating-body effects. In some cases, there are unique SOI material-to-process interactions that can cause yield loss if not properly modified and optimized. We have adjusted for interactions in shallow-trench isolation, transistor implants, salicidation, contact formation, and even the back-end-of-line (BEOL).

Around 1996, SOI technology development was being done on Motorola's most advanced CMOS platform. Feasibility demonstrations were performed using a 603 eV PowerPC microprocessor and a 4-Mbit asynchronous SRAM in 0.35µm and 0.22µm generations, respectively. That work showed SOI yield could be equivalent to bulk at improved speed and power. Motorola now has production and/or development in 0.1µm 0.13 µm , 90 nm and 65 nm SOI technologies. The 0.18 µm SOI technology in mass production offers core N and PMOS floating-body transistors, body-tied N/P-FETs, implanted precision resistors, zero-Vt NFETs, lateral P+/N well diodes, and N+/N well thin-oxide decoupling capacitors.

Performance up

In the more advanced technologies, we have added multiple Vts, additional precision passives, dual- or triple-gate oxide thicknesses, and up to nine levels of copper metal with low k dielectrics to expand to more system-on-chip applications. Transistor performance is generally 15-20 percent better than the equivalent bulk node. Our highest performance devices in the 90 nm technology boast sub-6 psecond/stage unloaded inverter delay with well-controlled transient effects.

We have successfully introduced multiple SOI technologies into manufacturing. Run rates are high, and can frequently exceed 1,000 wafers per week. Yields in all our production SOI technologies match or slightly exceed the equivalent bulk numbers. For the most part, yield limiters are similar to those of the bulk process. However, a small number of SOI-specific materials defects are still apparent. These are "large-area defects" usually caused by wafer-bonding voids and can show up as a circular cluster of failed bits in bit-mapped memories.



SOI offers the opportunity to combine a variety of n- and p- type MOSFETs with up to nine copper metal layers. Combined with low-k dielectrics, and added features such as multiple voltage thresholds and precision passive

devices, the materials system can realize between 15 and 20 percent better performance than bulk silicon alone.
Source: Motorola Inc.

In late 2001, Motorola began shipping the MPC7455 SOI microprocessor. This product is a member of Motorola's fourth-generation (G4) PowerPC family, and is derived from the original MPC7450, which was implemented in bulk silicon. It is manufactured in our 0.18 µm SOI technology featuring 65-nm gate lengths and six levels of copper interconnect. Initial SOI silicon showed a 20 percent speedup over bulk. The MPC7455 processor core supports a seven-stage pipeline, 11 execution units, and a memory subsystem that includes a 256-kbyte on-chip L2 cache. There are also on-chip L3 tag/status arrays to support the construction of an external L3 cache. The MPC7455 design includes 33 million transistors.

With over 750,000 parts shipped to-date, it represents a significant milestone for SOI. This SOI microprocessor has been recognized as "Best High-Performance Embedded Processor Chip" for 2001 by Microprocessor Report. The design currently supports frequencies up to 1.25 GHz. Certainly there is a long list of novel devices enabled by an SOI substrate or where the final device structure has both a front and back oxide. Today's planar CMOS SOI is a good stepping stone for novel devices and 3-D integration because the infrastructure, built for modeling and designing with floating-body devices, is highly leveraged.